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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/620,086	07/14/2003	Norio Sakai	M1071.1854/P1854	7417

7590 12/29/2005

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EXAMINER	
THOMAS, ERIC W	

ART UNIT	PAPER NUMBER
2831	

DATE MAILED: 12/29/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/620,086	SAKAI, NORIO	
	Examiner	Art Unit	
	Eric Thomas	2831	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *14 November 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *18-25* is/are pending in the application.

4a) Of the above claim(s) *22-25* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *18-21* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *14 July 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☒ Certified copies of the priority documents have been received in Application No. 09372547.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *6/05, 10/05*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Election/Restrictions

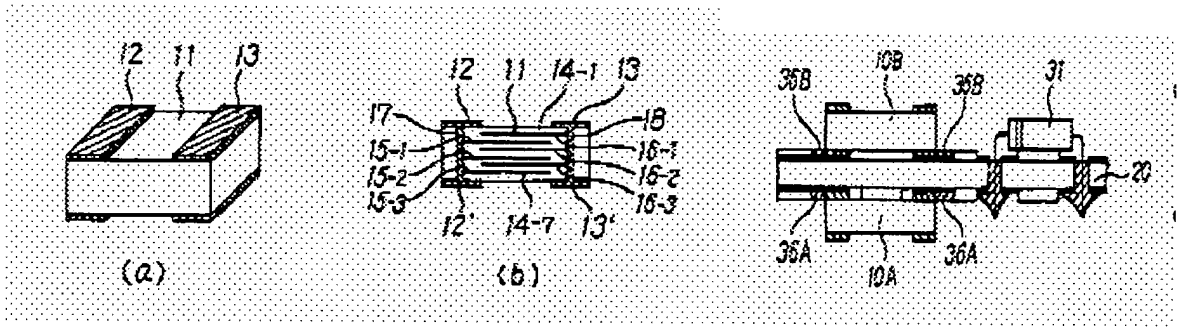
1. Claims 22-25 are withdrawn from further consideration pursuant to 37 CFR 1.142(b) as being drawn to a nonelected invention, there being no allowable generic or linking claim. Election was made **without** traverse in the reply filed on 11/14/05.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claims 18-20 are rejected under 35 U.S.C. 102(b) as being anticipated by 7-201634 ('634).



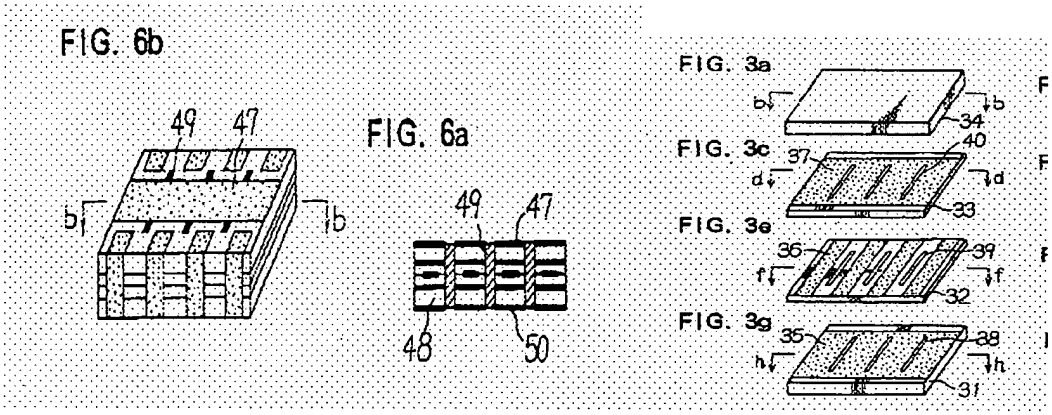
'634 discloses in fig. 2a, 2b, 5, a chip capacitor comprising: a multilayer body including a plurality of stacked ceramic sheet layers (14); a plurality of inner electrodes (15, 16) disposed within the multilayer body; a plurality of connectors (17, 18) disposed within the multilayer body so as to electrically connect the plurality of inner electrodes to each other; and a plurality of strip electrodes (12, 13) formed on outer main surfaces of

the multilayer body and electrically connected to some of the inner electrodes via corresponding connectors of the plurality of connectors, wherein a surface in a longitudinal direction of the multilayer body is a mounting surface of the chip capacitor for mounting to a printed circuit board (20).

Regarding claim 19, '099 disclose each connector of the plurality of connectors includes an aperture extending between the outer main surfaces, the aperture substantially being filled with a conductive material.

Regarding claim 20, '099 discloses wherein different connectors of the plurality of connectors electrically couple adjacent inner electrodes to each other.

4. Claims 18-21 are rejected under 35 U.S.C. 102(b) as being anticipated by Fujishiro et al. (US 5,590,016).



Fujishiro et al disclose in fig. 3, 6 a chip capacitor comprising: a multilayer body including a plurality of stacked ceramic sheet layers (31-34); a plurality of inner electrodes (35-37) disposed within the multilayer body; a plurality of connectors (45) disposed within the multilayer body so as to electrically connect the plurality of inner electrodes to each other; and a plurality of strip electrodes (47,50) formed on outer main

surfaces of the multilayer body and electrically connected to some of the inner electrodes via corresponding connectors of the plurality of connectors, wherein a surface in a longitudinal direction of the multilayer body is a mounting surface of the chip capacitor for mounting to a printed circuit board.

Regarding claim 19, Fujishiro et al disclose each connector of the plurality of connectors includes an aperture extending between the outer main surfaces, the aperture substantially being filled with a conductive material.

Regarding claim 20, Fujishiro et al disclose wherein different connectors of the plurality of connectors electrically couple adjacent inner electrodes to each other.

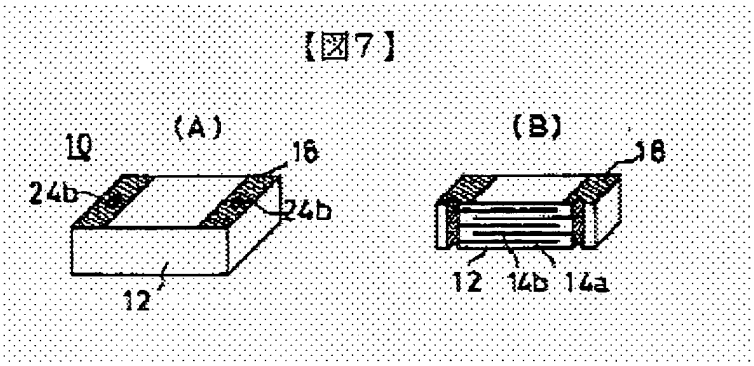
Regarding claim 21, Fujishiro et al disclose at least one of the inner electrodes is in the form of a strip line.

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claims 18-20 are rejected under 35 U.S.C. 103(a) as being unpatentable over JP 6-112099) in view of Monsorno (US 5,576,926).



'099 discloses in fig. 7a, 7b, a chip capacitor comprising: a multilayer body including a plurality of stacked ceramic sheet layers; a plurality of inner electrodes (14a, 14b) disposed within the multilayer body; a plurality of connectors (24b) disposed within the multilayer body so as to electrically connect the plurality of inner electrodes to each other; and a plurality of strip electrodes (18) formed on outer main surfaces of the multilayer body and electrically connected to some of the inner electrodes via corresponding connectors of the plurality of connectors.

'099 discloses the claimed invention except for a surface in a longitudinal direction of the multilayer body is a mounting surface of the chip capacitor for mounting to a printed circuit board.

Monsorno teaches that its known in the capacitor art to mount a chip capacitor to a printed circuit board, wherein a surface in a longitudinal direction of the multilayer body is a mounting surface of the chip capacitor for mounting to printed circuit board.

It would have been obvious to a person of ordinary skill in the art at the time the invention was made to form the capacitor of '099 on a printed circuit board, wherein a surface in a longitudinal direction of the multilayer body is a mounting surface of the chip capacitor for mounting to the printed circuit board, since such a modification would

provide a system for the capacitor to operate, and would provide a system with a capacitor having improved mounting and electrical characteristics.

Regarding claim 19, '099 discloses each connector of the plurality of connectors includes an aperture extending between the outer main surfaces, the apertures substantially being filled with a conductive material.

Regarding claim 20, '099 discloses wherein different connectors of the plurality of connectors electrically couple adjacent inner electrodes to each other.

Double Patenting

7. The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. A nonstatutory obviousness-type double patenting rejection is appropriate where the conflicting claims are not identical, but at least one examined application claim is not patentably distinct from the reference claim(s) because the examined application claim is either anticipated by, or would have been obvious over, the reference claim(s). See, e.g., In re Berg, 140 F.3d 1428, 46 USPQ2d 1226 (Fed. Cir. 1998); In re Goodman, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); In re Longi, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); In re Van Ornum, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); In re Vogel, 422 F.2d 438, 164 USPQ 619 (CCPA 1970); and In re Thorington, 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) or 1.321(d) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent either is shown to be commonly owned with this application, or claims an invention made as a result of activities undertaken within the scope of a joint research agreement.

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

8. Claims 18-21 are rejected on the ground of nonstatutory obviousness-type double patenting as being unpatentable over claims 1, 10 of U.S. Patent No. 6381120 in view of JP 7-201634 ('634).

Regarding claim 18, '120 discloses a chip capacitor comprising: a multilayer body including a plurality of stacked ceramic sheet layers; a plurality of inner electrodes disposed within the multilayer body; a plurality of connectors disposed within the multilayer body so as to electrically connect the plurality of inner electrodes to each other; and a plurality electrodes formed on outer main surfaces of the multilayer body and electrically connected to some of the inner electrodes via corresponding connectors of the plurality of connectors.

'120 discloses the claimed invention except for the outer main surface electrodes are strips and the surface in a longitudinal direction of the multilayer body is a mounting surface of the chip capacitor for mounting on a printed circuit board.

'634 teaches that it is known to form outer main surface electrodes into strips and the surface in a longitudinal direction of the multilayer body is a mounting surface of the chip capacitor for mounting on a printed circuit board.

It would have been obvious to a person of ordinary skill in the art at the time the invention was made to form the capacitor of '634 on a printed circuit board wherein a surface in a longitudinal direction of the multilayer body is a mounting surface of the chip capacitor for mounting to the printed circuit board and form the mounting surface electrode in strips, since such a modification would provide a system for the capacitor to operate, and would provide a system with a capacitor having improved mounting and electrical characteristics.

Regarding claim 19, '120 discloses each connector of the plurality of connectors includes an aperture extending between the outer main surfaces, the aperture substantially being filled with a conductive material.

Regarding claim 20, '120 discloses different connectors of the plurality of connectors electrically couple adjacent inner electrodes to each other.

Regarding claim 21, '120 discloses at least one of the inner electrodes is in the form of a strip line.

9. Claims 18-21 are rejected on the ground of nonstatutory obviousness-type double patenting as being unpatentable over claims 1, 7 of U.S. Patent No. 6,236,558 ('558) in view of JP 7-201634 ('634).

Regarding claim 18, '558 discloses a chip capacitor comprising: a multilayer body including a plurality of stacked ceramic sheet layers; a plurality of inner electrodes disposed within the multilayer body; a plurality of connectors disposed within the multilayer body so as to electrically connect the plurality of inner electrodes to each other; and a plurality electrodes formed on outer main surfaces of the multilayer body and electrically connected to some of the inner electrodes via corresponding connectors of the plurality of connectors.

'558 discloses the claimed invention except for the outer main surface electrodes are strips and the surface in a longitudinal direction of the multilayer body is a mounting surface of the chip capacitor for mounting on a printed circuit board.

'634 teaches that it is known to form outer main surface electrodes into strips and the surface in a longitudinal direction of the multilayer body is a mounting surface of the chip capacitor for mounting on a printed circuit board.

It would have been obvious to a person of ordinary skill in the art at the time the invention was made to form the capacitor of '634 on a printed circuit board wherein a surface in a longitudinal direction of the multilayer body is a mounting surface of the chip capacitor for mounting to the printed circuit board and form the mounting surface electrode in strips, since such a modification would provide a system for the capacitor to operate, and would provide a system with a capacitor having improved mounting and electrical characteristics.

Regarding claim 19, '558 discloses each connector of the plurality of connectors includes an aperture extending between the outer main surfaces, the aperture substantially being filled with a conductive material.

Regarding claim 20, '558 discloses different connectors of the plurality of connectors electrically couple adjacent inner electrodes to each other.

Regarding claim 21, '558 discloses at least one of the inner electrodes is in the form of a strip line.

Conclusion

10. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

JP 10-12491 – Discloses a capacitor having an internal inductor element.

5,815,367 – English equivalent of JP 10-12491.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Eric Thomas whose telephone number is 571-272-1985. The examiner can normally be reached on Monday - Friday 6:30 AM - 3:45 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Dean Reichard can be reached on 571-272-1984. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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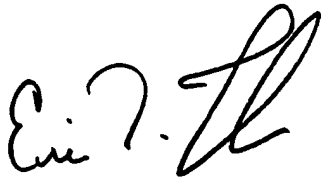

ERIC W. THOMAS
PRIMARY EXAMINER